

Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

- 1 1. (currently amended) A system for processing simplex and multiplexed voice packets,
2 comprising:
3 a compare circuit that includes a plurality of locations that include
4 simplex entries and multiplex entries, each simplex entry including data that
5 can match simplex packet information and indicia for identifying a simplex
6 entry, each multiplex entry including data that can match multiplex packet
7 information and indicia for identifying a multiplex entry.

1 2. (original) The system of claim 1, wherein:
2 each simplex entry includes data that can match predetermined
3 simplex packet header information.

1 3. (original) The system of claim 1, wherein:
2 each simplex entry includes data that can match information
3 corresponding to at least one network layer.

1 4. (original) The system of claim 1, wherein:
2 each simplex entry includes data that can match a user datagram
3 protocol destination port address.

1 5. (original) The system of claim 1, wherein:
2 each simplex and multiplex entry includes an entry type field having a
3 first value in a simplex entry and a second value different from the first value
4 in a multiplex entry.

1 6. (original) The system of claim 1, wherein:
2 the compare circuit includes a content addressable memory (CAM).

1 7. (original) The system of claim 6, wherein:
2 the CAM includes maskable entries.

1 8. (original) The system of claim 7, wherein:
2 the CAM entries are globally maskable.
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2 9. (presently amended) A packet processing system, comprising:
3 a compare section having a content addressable memory (CAM) that
4 includes a plurality of entries that match simplex voice packet information and
5 multiplexed voice packet information each entry including at least one bit that
6 indicates if the entry matches simplex voice packet information or multiplexed
7 voice packet information.

1 10. (Cancelled)

1 11. (original) The packet processing system of claim 9, wherein:
2 each entry that matches multiplexed voice packet information includes
3 a field that stores a voice channel value.

1 12. (original) The packet processing system of claim 11, wherein:
2 each entry that matches multiplexed voice packet information further
3 includes a trunk field that stores a data value corresponding to a grouping of
4 voice channels.

1 **13.** (original) The packet processing system of claim 9, wherein:

2 each entry that matches simplex voice packet information includes a
3 field that stores a voice channel value.

1 **14.** (original) The packet processing system of claim 9, wherein:

2 each entry that matches simplex voice packet information includes a
3 field that matches transport layer header information.

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2 **15.** (original) A system, comprising:

3 a processor;

4 a storage register coupled to the processor that stores simplex voice
5 packet information;

6 a voice packet input coupled to the processor that provides multiplexed
7 voice packet information; and

8 a compare circuit coupled to the processor that compares simplex
9 voice packet information from the storage register and multiplexed voice
10 packet information from the voice packet input to a plurality of entries, each
11 entry indexing to a particular voice channel.

1 **16.** (original) The system of claim 15, wherein:

2 the compare circuit includes a content addressable memory (CAM).

1 **17.** (original) The system of claim 16, wherein:

2 each CAM entry includes at least one entry type field for
3 distinguishing between entries that match simplex voice packet information
4 and entries that match multiplexed voice packet information.

1 **18.** (original) The system of claim 17, wherein:

2 each entry indexes address information for a storage location
3 corresponding to a voice channel.

1 **19.** (original) The system of claim 15, wherein:

2 the compare circuit entries each include valid indications that indicate
3 when an entry contains valid information.

1 **20.** (original) The system of claim 15, wherein:

2 the compare circuit compares simplex voice information with multiple
3 entries.

1 **21.** (original) The system of claim 15, wherein:

2 the compare circuit compares multiplex voice information with
3 multiple entries.